a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulting film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed throughout a portion below at least one of said power supply line and ground line.

REMARKS

Favorable reconsideration of the above-identified patent application in light of the following remarks is respectfully requested.

Claim 1 is active in the application; Claims 2-20 are withdrawn from consideration.

In the Office Action dated June 6, 2002, the restriction requirement was made final, and Claim 1 was rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,747,846 (Iida *et al.*).

Applicants traverse the rejection.

Applicants respectfully submit that the Iida *et al.* patent does not disclose or suggest the particular combination of elements recited in Claim 1:

> 1. (Amended) A semiconductor device comprising:
> an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;
> a partial-isolation insulating film formed in a main surface of said semiconductor layer.
> a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulting film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and ***a ground line*** formed on said interlayer insulating film; and

a first ***complete-isolation insulating film formed throughout a portion below at least one of said power supply line and ground line.*** (emphasis added)

Various claimed features are not disclosed in the Iida *et al.* patent as interpreted according to the June 6, 2002 Office Action.

First, Claim 1 requires the presence of "at least one of a power supply line and a ground line formed on said interlayer insulating film." The Office Action does not mention anything corresponding to a power supply line, but attempts to correlate Iida's bit line B1 and aluminum electrode 53 with the claimed "ground line." However, the passage in the Iida *et al.* patent to which the examiner refers[1] is part of an explanation[2] of the programming, erasing and reading operations of Iida's memory cell. In particular, the specific passage to which the Office Action refers based on a premise that a particular *signal*, which happens to be at ground level at certain times, may be applied to bit line B1 (see column 5, lines 2-7, especially lines 5-6: "a ground potential is applied to the bit line B of a cell into which 1 is to be written..."). Thus, Applicants submit that this disclosure shows that Iida's bit line B1 may *on occasion* be held at ground level, but is not, as claimed, an actual "ground line" as would reasonably be understood by those skilled in the art. Accordingly, neither a power supply line, nor an actual "ground line" as reasonably understood by those skilled in the art, are disclosed or taught by the Iida *et al.* patent in the context of the present invention.

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[1]Iida *et al.*; column 5, lines 8-16.

[2]Id., column 4, line 54 *et seq.*

Those skilled in the art would interpret the term "ground line" to mean a line that connects a semiconductor element to a *fixed* ground potential. As a non-limiting example supporting Claim 1's "ground line," the examiner is referred to Applicants' element 22 (FIGS. 1, 17, 19), which is connected to a source region 28 of an NMOS transistor. Generally, source electrodes of NMOS transistors in CMOS inverters are connected to a *fixed* ground potential, a connection accomplished by element 22. Accordingly, there is basis in both common usage in the art, and in Applicants' own specification, for interpreting Claim 1's "ground line" as a line that connects a semiconductor element to a *fixed* ground potential.

Second, Claim 1 requires that the complete-isolation insulating film be formed throughout a portion below at least one of said power supply line and ground line. This limitation cannot be met due to the observation noted above, that Iida *et al.* do not disclose a power supply line or a ground line as would reasonably be interpreted by those skilled in the art. By implication, no complete-isolation insulating film can be formed below such a line if such a line does not exist.

As a non-limiting example of Claim 1's complete-isolation insulating film, the examiner is referred to 23 (FIGS. 1,2 19, 20) that is formed throughout a portion below a *power supply* line, and to element 51 (FIGS. 17-20) that is formed throughout a portion below a *ground* line. In contrast to Applicants' Claim 1, Iida's arrangement includes a portion below line 53 where a complete-isolation insulation film (presumably elements 8, 13) is not formed. Accordingly, the Iida *et al.* patent does not fulfill Claim 1's requirement that the complete-isolation insulating film be formed "throughout a portion below at least one of said power supply line and ground line."

Either or both of the foregoing reasons demonstrate that Claim 1, especially as amended, clearly and patentably distinguishes the invention over the Iida *et al.* patent. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

In light of the foregoing discussion, it is respectfully submitted that Claim 1 is allowable and that the case is in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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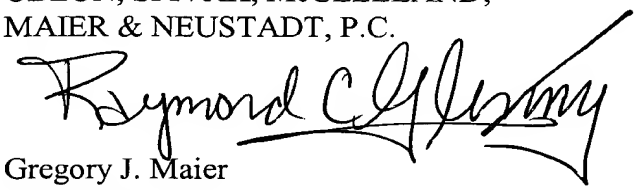

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ATTACHMENT

SHOWING CHANGES TO APPLICATION

1. (Amended) A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

a partial-isolation insulating film formed in a main surface of said semiconductor layer.

a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulting film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed throughout a portion [extending from said main surface of said semiconductor layer, reaching an upper surface of said insulating layer] below at least one of said power supply line and ground line.